

PAT-NO: JP401251791A  
DOCUMENT-IDENTIFIER: JP 01251791 A  
TITLE: MANUFACTURE OF WIRING BOARD  
PUBN-DATE: October 6, 1989

INVENTOR-INFORMATION:

NAME

IWASAKI, YORIO  
FUKUTOMI, NAOKI  
NAKAMURA, HIDEHIRO  
ARIGA, SHIGEHARU  
KOJIMA, FUJIO

ASSIGNEE-INFORMATION:

NAME

HITACHI CHEM CO LTD

COUNTRY

N/A

APPL-NO: JP63078425  
APPL-DATE: March 31, 1988

INT-CL (IPC): H05K003/46  
US-CL-CURRENT: 427/FOR.106

ABSTRACT:

PURPOSE: To make a high-density wiring using a 0.10mm wire and to obtain a multiwire wiring board which meets a condition  $Z_0$ (impedance)=50ohms and has an excellent insulation deteriorating property, by covering a recessed portion of an insulating board, on which an inner circuit is formed, with material which is made by mixing several kinds of resins in specific proportions.

CONSTITUTION: A gland circuit 3 is formed as a power supply on an insulating board 2. A compound of 10~50 pts.wt. epoxy resin whose molecular weight is

5,000 or more, 5~25 pts.wt. alkylmelamine resin, 5~50 pts.wt. saturated polyester and 10~40 pts.wt. inorganic fiber filler as against 100 pts.wt. epoxy resin whose molecular weight is less than 5,000 and a crosslinking agent are dissolved in a mixed solvent, dispersed, coated on a separation film and cured to a state of B stage. This is placed on an inner circuit board 1 and is applied with pressure and heat with an end plate piled on it, to form a resin layer 4 with a smooth surface. Next, an adhesive resin layer 5 is laminated, on the surface of which, a wire 6 is adhered to a desired wiring pattern. Then, a thermosetting resin layer 7 is formed and a hole is made. On an inner surface of the hole, a through-hole copper-plated layer 8 is formed.

COPYRIGHT: (C)1989, JPO&Japio